

APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: ANTENNA SELECTION FOR DIVERSITY COMBINING

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BACKGROUND OF THE INVENTION

[0001] Many wireless communication systems may use more than one antenna for diversity. In such cases, the receiver apparatus may choose to process the output of one antenna (for example, it may choose to process the "best" signal out of any of the antennas; criteria for choosing a "best" signal may include, but are not limited to, signal-to-noise ratio, received signal strength, noise level, etc.). Alternatively, if there are multiple receiver chains in the receiver apparatus, each of the multiple receiver chains may process the output of a particular antenna. The outputs of these receiver chains may then be combined according to some analog or digital combining method, which may result in improved reception.

[0002] Some receive apparatuses may include more antennas than receiver chains. In such a case, it is necessary to choose to which antennas the receiver chains should be coupled for processing the signals from the antennas.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Preferred embodiments of the invention will now be described in connection with the associated drawings, in which:

[0004] Figure 1 depicts a conceptual block diagram of a system implementing a first exemplary embodiment of the invention;

[0005] Figure 2 depicts a conceptual block diagram of a system implementing a second exemplary embodiment of the invention;

[0006] Figure 3 depicts a conceptual block diagram of a system implementing a third exemplary embodiment of the invention;

[0007] Figure 4 depicts a conceptual block diagram of a system implementing a fourth exemplary embodiment of the invention;

[0008] Figure 5 depicts a conceptual block diagram of a system implementing a fifth exemplary embodiment of the invention;

[0009] Figure 6 depicts a conceptual block diagram of a system implementing a sixth exemplary embodiment of the invention;

[0010] Figure 7 depicts a conceptual block diagram of a system implementing a seventh exemplary embodiment of the invention;

[0011] Figure 8 depicts a conceptual block diagram of a further implementation of an embodiment of the invention; and

[0012] Figure 9 depicts a conceptual block diagram of a system implementing a further embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0013] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures, and/or techniques have not been shown in detail in order not to obscure an understanding of this description.

[0014] References to “one embodiment”, “an embodiment”, “example embodiment”, “various embodiments”, etc., indicate that the embodiment(s) of the invention so described may include a particular feature, structure, or characteristic, but not every

embodiment necessarily includes the particular feature, structure, or characteristic.

Further, repeated use of the phrase “in one embodiment” does not necessarily refer to the same embodiment, although it may.

[0015] In the following description and claims, the terms “coupled” and “connected,” along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, “connected” may be used to indicate that two or more elements are in direct physical or electrical contact with each other. “Coupled” may mean that two or more elements are in direct physical or electrical contact. However, “coupled” may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

[0016] An algorithm is here, and generally, considered to be a self-consistent sequence of acts or operations leading to a desired result. These include physical manipulations of physical quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers or the like. It should be understood, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities.

[0017] Unless specifically stated otherwise, as apparent from the following discussions, it is appreciated that throughout the specification discussions utilizing terms such as “processing,” “computing,” “calculating,” “determining,” or the like, refer to the action

and/or processes of a computer or computing system, or similar electronic computing device, that manipulate and/or transform data represented as physical, such as electronic, quantities within the computing system's registers and/or memories into other data similarly represented as physical quantities within the computing system's memories, registers or other such information storage, transmission or display devices.

[0018] In a similar manner, the term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory. A "computing platform" may comprise one or more processors.

[0019] Embodiments of the present invention may include apparatuses for performing the operations herein. An apparatus may be specially constructed for the desired purposes, or it may comprise a general purpose device selectively activated or reconfigured by a program stored in the device.

[0020] Embodiments of the invention may be implemented in one or a combination of hardware, firmware, and software. Embodiments of the invention may also be implemented as instructions stored on a machine-readable medium, which may be read and executed by a computing platform to perform the operations described herein. A machine-readable medium may include any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium may include read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.), and others.

[0021] Figure 1 depicts a conceptual block diagram including an exemplary implementation of an embodiment of the invention. A receiver system according to an embodiment of the invention may include multiple antennas 1 (1a, 1b, 1c, 1d) connected to a switch 2. Switch 2 is also connected to two or more receiver chains, two of which, 7a and 7b, are shown in the figure. A receiver chain, for example, 7a, may comprise one or more of a low noise amplifier (LNA) 3a, automatic gain control (AGC) 4a, a mixer 5a, and an analog-to-digital converter (ADC) 6a. Each of receiver chains 7a and 7b may be connected to a combiner 8 adapted to combine the outputs of receiver chains 7a and 7b according to a diversity combining method. One example of such a diversity combining method, to which the invention is not limited, is maximal ratio combining. Following diversity combining 8, normal demodulation and/or decoding 9 may be performed on the resulting (combined) signal. By using switch 2, two signals, which may be selected according to some predetermined criterion or criteria (examples of which may be, but are not limited to, signal-to-noise ratio, received signal strength, and noise level), may be selected for processing in receiver chains 7a and 7b.

[0022] In Figure 1, combiner 8 is shown connected following ADCs 6a and 6b. However, in an alternative embodiment, combiner 8 may be connected to analog signals (i.e., prior to ADCs 6a and 6b), and a single ADC may be used, after combining, to convert the analog signal to a digital signal. Alternatively, if demodulator/decoder 9 is designed to be capable of handling analog signals, it may be possible to omit ADCs altogether.

[0023] A further embodiment of the invention is shown in Figure 2, which includes a first embodiment of switch 2. In this embodiment, switch 2 may comprise two 4x2 sub-

switches, each adapted to couple one of the receiver chains 7a, 7b to any one of the antennas 1. In a more general setting, in which there are K antennas and N receiver chains, this would be equivalent to using N Kx1 sub-switches. In this arrangement, any receiver chain 7a, 7b may be connected to any one of the antennas 1.

[0024] The embodiment of Figure 2 may further include a power amplifier 10, typically used for transmission. To accommodate transmission, the switch 2 may further include a 4x1 sub-switch adapted to couple the output of power amplifier 10 to any one of the four antennas 1. Such an arrangement may be useful, for example, if switch 2 is included as part of a transceiver.

[0025] Figure 3 shows a further embodiment of the invention. In this embodiment, switch 2 may comprise two 3x1 sub-switches, each adapted to switch three of the four antenna outputs to one of the receiver chains 7a, 7b. For example, as shown in Figure 3, one 3x1 switch may be adapted to couple one of antennas 1a, 1b, and 1c to receiver chain 7a, and the other 3x1 sub-switch may be adapted to couple one of antennas 1b, 1c, and 1d to receiver chain 7b. Note that this is merely an exemplary arrangement, and the invention is not to be understood as being limited to this arrangement. Switch 2 may further include a 4x1 sub-switch, as in the previous embodiment, adapted to couple the output of power amplifier 10 to one of the four antennas 1.

[0026] In the embodiment of Figure 3, although each receiver chain 7a, 7b may not be capable of being coupled to every antenna 1, the switching arrangement is such that each receiver chain 7a, 7b may be coupled to a different one of the antennas 1 in such a way that all combinations of two of the four antennas 1 may be received.

[0027] The embodiment of Figure 3 may be generalized to the case of K antennas and N receiver chains. In that case, switch 2 may comprise $N (K-N+1) \times 1$ sub-switches, each coupled to one of the N receiver chains and adapted to couple a particular receiver chain with one of $K-N+1$ of the K antennas.

[0028] Figure 4 shows a further embodiment of the invention. In this embodiment, switch 2 may comprise a cascaded switching arrangement, which may comprise switches 2a and 2b. Switch 2a may comprise a 3×1 sub-switch and a 4×1 sub-switch, while switch 2b may comprise a 2×1 switch that may be coupled to the 4×1 sub-switch. In this arrangement, switch 2b may be coupled to power amplifier 10 and a receiver chain 7b. Switch 2b may be adapted to couple one of power amplifier 10 and receiver chain 7b to the 4×1 sub-switch of switch 2a. The 4×1 sub-switch of switch 2a may, in turn, be adapted to couple either power amplifier 10 or receiver chain 7b (whichever is coupled to the 4×1 sub-switch by 2×1 switch 2b) to one of the four antennas 1. The 3×1 sub-switch of switch 2a may be adapted to couple receiver chain 7a to one of three of the four antennas, for example, but not limited to, antennas 1a, 1b, and 1c. As in the embodiment of Figure 3, although each receiver chain 7a, 7b in the embodiment of Figure 4 may not be capable of being coupled to every antenna 1, the switching arrangement is such that each receiver chain 7a, 7b may be coupled to a different one of the antennas 1 in such a way that all combinations of two of the four antennas 1 may be received.

[0029] Note that the embodiment of Figure 4 may be generalized for the case of K antennas and N receiver chains. In such a case, $N-1$ of the receiver chains may be coupled to one of $K-1$ of the K antennas via $(N-1) (K-1) \times 1$ sub-switches in switch 2a,

while a power amplifier and an Nth receiver chain may be coupled to a 2x1 switch 2b coupled to a Kx1 sub-switch in switch 2a.

[0030] The embodiment of Figure 4 may allow for a simpler switching structure than the embodiments of Figures 2 and 3. On the other hand, use of a cascaded switch network may introduce an insertion loss. In general, however, such insertion loss may be rather small (for example, on the order of 0.4 dB for signals in the 0-6 GHz band).

[0031] Figure 5 shows another embodiment of the invention that may employ cascaded switching. In this embodiment, a receiver chain 7b and power amplifier 10 may be, once again, coupled to switch 2a by a 2x1 switch 2b. In this embodiment, however, switch 2a may comprise a 4x1 sub-switch, which may be coupled to switch 2b, and a 2x1 sub-switch, which may be coupled to receiver chain 7a. In this fashion, either power amplifier 10 or receiver chain 7b may be coupled to any of the antennas 1. On the other hand, receiver chain 7a may only be coupled to one of two of the four antennas 1; in Figure 5, these two antennas would be antennas 1a and 1b (however, this is merely an example, and the invention is not to be understood as being limited to this case). As a result, in the exemplary implementation shown in Figure 5, all combinations of two antennas may be connected to receiver chains 7a and 7b except for one, the combination of antennas 1c and 1d. As a result, the switching arrangement of Figure 5 may be simpler, but it may also be sub-optimal, as one possible combination of antennas may be impossible to achieve.

[0032] As in the previous embodiments, the embodiment of Figure 5 may be generalized to the case of K antennas and N receiver chains, if desired. Furthermore, as discussed

above in connection with the embodiment of Figure 4, the use of cascaded switching may add an additional insertion loss.

[0033] Figure 6 shows another embodiment of the invention, without cascaded switching. In this embodiment, switch 2 may have separate sub-switches for each receiver chain 7a, 7b and for power amplifier 10. In the illustrated embodiment, the switch connected to power amplifier 10 may be a 4x1 sub-switch, which may permit power amplifier 10 to be coupled to any of the four antennas 1. Each receiver chain 7a, 7b may be coupled to a 2x1 sub-switch in switch 2, which thus may permit each of the receiver chains 7a, 7b to be coupled to one of two of the four antennas 1. In Figure 6, receiver chain 7a may be coupled to antenna 1a or antenna 1b, while receiver chain 7b may be coupled to antenna 1c or antenna 1d. Note that these couplings are exemplary, and the invention is not to be thus limited. In this example, therefore, receiver chains 7a, 7b may be coupled to the combinations of antennas {(1a, 1c), (1a, 1d), (1b, 1c), (1b, 1d)}, but they may not be coupled to the combinations {(1a, 1b), (1c, 1d)}. As a result, two possible combinations of antennas may not be possible to achieve.

[0034] Again, as in the previous embodiments, the embodiment of Figure 6 may be generalized to K antennas and N receiver chains.

[0035] Figure 7 shows an exemplary implementation of a further embodiment of the invention in which there may be K antennas and K-1 receiver chains. As shown in the exemplary implementation of Figure 7, there may be four antennas 1 and three receiver chains 7a, 7b, 7c. In this case, switch 2 may comprise three 2x1 sub-switches, each coupled to one of receiver chains 7a, 7b, 7c, and one 4x1 sub-switch, coupled to power amplifier 10. In such an arrangement, power amplifier 10 may be coupled to any of the

four antennas 1, and each of the receiver chains 7a, 7b, 7c may be connected to two of the four antennas 1. Using this arrangement of switches, it may be possible to choose any three antennas out of the four antennas 1 for processing by the three receiver chains 7a, 7b, 7c.

[0036] When generalizing the embodiment of Figure 7 for K antennas and K-1 receiver chains, switch 2 may comprise K-1 2x1 sub-switches, each of which may be coupled to one of the K-1 receiver chains.

[0037] The above embodiments may be used in either symmetric or asymmetric uplink-downlink combinations. Here, a symmetric combination is one in which both the uplink and the downlink employ the same diversity arrangement in their receivers, which, for example, may be as discussed in one of the above embodiments. An asymmetric combination is one in which the uplink and downlink receivers differ in their diversity arrangements. Because diversity may generally result in a processing gain, in an asymmetric channel, the diversity processing gain may exist in one direction and not in the other (or there may be different processing gains).

[0038] As an example, as shown in Figure 9, a channel may have a transceiver 91 at one end that may employ diversity resulting in a processing gain of, for example, 9 dB (in effective signal-to-noise ratio), while the transceiver 92 at the other end of the channel may employ no diversity. The transceiver 91 using diversity may use the knowledge of this processing gain difference to reduce its transmit data rate to compensate for its counterpart transceiver 92 that lacks the same processing gain. In other words, the transceiver with diversity 91 may reduce its data rate such that a necessary signal-to-noise ratio to support a desired symbol (or bit) error rate may be reduced by 9 dB (using

the example above; this should not be understood as limiting the scope of the invention), corresponding to the lack of processing gain in the transceiver lacking diversity 92. The amount of such data rate back-off may be determined, for example, using well-known methods of computing error rates as functions of signal-to-noise ratios.

[0039] The above algorithm may also use information on, for example, number of antennas and/or transceiver chains, output power, and/or receiver sensitivity. Such information may, for example, be exchanged between transceivers when a communication link is established.

[0040] Some embodiments of the invention, as discussed above, may be embodied in the form of software instructions on a machine-readable medium. Such an embodiment is illustrated in Figure 8. The computer system of Figure 8 may include at least one processor 82, with associated system memory 81, which may store, for example, operating system software and the like. The system may further include additional memory 83, which may, for example, include software instructions to perform various applications. The system may also include one or more input/output (I/O) devices 84, for example (but not limited to), keyboard, mouse, trackball, printer, display, network connection, etc. The present invention may be embodied as software instructions that may be stored in system memory 81 or in additional memory 83. Such software instructions may also be stored in removable or remote media (for example, but not limited to, compact disks, floppy disks, etc.), which may be read through an I/O device 84 (for example, but not limited to, a floppy disk drive). Furthermore, the software instructions may also be transmitted to the computer system via an I/O device 84, for

example, a network connection; in such a case, a signal containing the software instructions may be considered to be a machine-readable medium.

[0041] Furthermore, the invention may be used in systems that include, but are not limited to, wireless local area networks (WLANs), cellular networks, personal communication networks, etc. The invention may be incorporated into transceivers, network interface cards (NICs), and the like, which are intended to be non-limiting examples.

[0042] The invention has been described in detail with respect to preferred embodiments, and it will now be apparent from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects. The invention, therefore, as defined in the appended claims, is intended to cover all such changes and modifications as fall within the true spirit of the invention.